Patent Claims

1. Process for producing an etching mask on a microstructure, in particular a semiconductor structure with one or more trench capacitors (5), which includes the following steps:

providing a lower first, a middle second and an upper third hard-mask layer (60; 70; 80) on a surface (O) of the microstructure, the third hard-mask layer (80) being significantly thinner than the first and second hard-mask layers (60; 70);

providing a photoresist mask (100) above the third hard-mask layer (80);

patterning the third hard-mask layer (80) by etching chemistry using the photoresist mask (100);

patterning the second hard-mask layer (70) by etching chemistry using the patterned third hard-mask layer (80), with the photoresist mask (100) being removed at the same time;

patterning the first hard-mask layer (60) by etching chemistry using the patterned second hard-mask layer (70), with the third hard-mask layer (80) being removed at the same time; and

removing the patterned second hard-mask layer (70).

2. Process according to Claim 1, characterized in that an antireflection coating (90) is provided between the third hard-mask layer (80) and the photoresist mask (100), which antireflection coating is patterned prior to the patterning of the third hard-mask layer (80) by

etching chemistry using the photoresist mask (100) and is removed during the patterning of the second hard-mask layer (70) by etching chemistry using the patterned third hard-mask layer (80).

3. Process according to Claim 1 or 2, characterized in that the first hard-mask layer (60) consists of borosilicate glass.

4. Process according to one of the preceding claims, characterized in that the second hard-mask layer (70) consists of a carbon-containing material, in particular of amorphous C:H.

5. Process according to one of the preceding claims, characterized in that the third hard-mask layer (80) consists of silicon oxynitride.

6. Process according to one of the preceding claims, characterized in that the second and third hard-mask layers (70; 80) are such that they can be structured by etching chemistry with a selectivity of greater than 100:1, in particular greater than 200:1.

7. Process according to one of the preceding claims, characterized in that the patterning of the first, second and third hard-mask layers (609; 70; 80) by etching chemistry is carried out sequentially in the same plasma-etching chamber.

8. Process according to one of the preceding claims, characterized in that the first and second hard-mask layers (60; 70) have a thickness of from 100 to 400 nm, in particular from 200 to 300 nm.

9. Process according to Claim 8, characterized in that the third hard-mask layer (80) has a thickness of from 10 to 40 nm, in particular from 20 to 30 nm.

10. Process according to one of the preceding claims, characterized in that the photoresist mask (100) has a thickness of less than or equal to 150 nm.

11. Process according to one of the preceding claims, characterized in that the microstructure is a semiconductor structure with one or more trench capacitors (5), on which there is a further hard mask (50) for the prior fabrication of the trench capacitor(s) (5), with filling of a capacitor filling (40), which is recessed with respect to the surface (O), of the trench capacitor(s) (5) being completed during the provision of the first hard-mask layer (60).

12. Use of an etching mask produced using the process according to Claim 11 for the fabrication of isolation trenches (STI) for isolating the trench capacitors (5), patterning of the further hard mask (50) by etching chemistry for the preceding fabrication of the trench capacitor(s) (5) taking place after the patterning of the first hard-mask layer (60) by etching chemistry using the patterned second hard-mask layer (70) and recessing of the first hard-mask layer (6) in regions down to the recessed capacitor filling (40) of the trench capacitor(s) (5).